WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate having a top surface and a bottom surface;

a ridge formed at the top surface of the substrate and comprising at least one layer of a semiconductor material, the ridge having a base attached to the substrate, an upper face located above the base, a first body section located between the base and the upper face, a second body section located between the first body section and the upper face, and at least a first side face located between the ridge's upper face and the base and located to one side of the first and second body sections, the first side face having a first area which spans over the first body section and a second area which spans over the second body section, the first side face further having a straight mesa slope or a forward mesa slope in the first area and a reverse mesa slope in the second area; and

a dielectric layer disposed on the first side face and covering the first area and at least a portion of the second area which is closest to the first area.

2. The semiconductor device of Claim 1, wherein the dielectric layer is disposed to cover the entire first and second areas.

3. The semiconductor device of Claim 1 wherein the top surface portion of the ridge comprises a material which is more resistance to plasma etching than the material of the dielectric layer.

4. The semiconductor device of Claim 1 further comprising a layer of conductive material disposed over the dielectric layer, the upper face of the ridge, and a portion of the second area of the first side face which is closest to the upper face of the ridge.

5. The semiconductor device of Claim 1 wherein the ridge has a base width (A3) along the cross-sectional width of the base, the base width having a value in a range of 2.7 μm to 4.5 μm;

wherein the ridge has a top width (A1) along the cross-sectional width of the ridge's top face, the top width having a value in the range of forty percent of the base width to sixty-five percent of the base width;

wherein the ridge has an interface plane between the first and second body sections of the ridge, wherein the ridge has a neck width (A2) along the cross-sectional width of the ridge at the interface plane, and wherein the neck width has a value in the range of eighty percent of the ridge top width to ninety-five percent of the ridge top width.

6. The semiconductor device of Claim 5 wherein the ridge has a first height (H10 from the base to the interface plane and a second height (H2) from the interface plane to the top surface of the ridge, wherein the first height has a value in the range of 1.3 μm to 1.4 μm, and wherein the second height has a value in the range of 0.4 μm to 0.6 μm.

7. The semiconductor device of Claim 1 further comprising a conductive layer disposed over a portion of the first side face at a first thickness (T_1) and an adjacent portion of the upper face of the ridge at a second thickness (T_2), said first thickness being equal to or greater than fifty percent of the second thickness, said conductive layer comprises one or more sublayers, each sublayer comprising a material which has less than 5% of gold by weight.

8. The semiconductor device of Claim 7 wherein said first thickness is greater than or equal to 150 nm.

9. The semiconductor device of Claim 7 wherein the first thickness is less than or equal to one-hundred and twenty percent of the second thickness.

10. The semiconductor device according to Claim 7, wherein the first thickness is equal to or greater than sixty percent of the second thickness.

11. The semiconductor device according to Claim 10, wherein the first thickness is less than or equal to said second thickness.

12. The semiconductor device according to Claim 7, wherein said first thickness is substantially equal to said second thickness.

13. The semiconductor device of Claim 1 further comprising a conductive layer disposed over a portion of the first side face at a first thickness (T_1) and an adjacent portion of the upper face of the ridge at a second thickness (T_2), said first thickness is greater than or equal to 150 nm, said conductive layer comprises one or more sublayers, each sublayer comprising a material which has less than 5% of gold by weight.